Remarks:

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of Applicants' claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is respectfully requested.

Claims 1 - 17 are presently pending in the application.

Of those claims, Applicants gratefully acknowledge that the Examiner has indicated that claims 7 and 9 are allowable, if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

However, claims 1 - 6, 8 and 10 - 17 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U. S. Patent No. 5,614,855 to Lee et al. ("**LEE**"). Applicants respectfully traverse the above rejection of these claims.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 recites, among other limitations, a method for generating a clock pulse in a data processing system **having a plurality of independent, non-synchronous digital data channels**. Independent claim 8 similarly recites, among other limitations, a configuration for generating a clock pulse in a

data processing system **having a plurality of independent, non-synchronous digital data channels.**

That the present invention relates to generating a clock pulse in a data processing system having a number of non-synchronous (i.e. asynchronous) data channels is clearly set forth throughout the specification of the present application. See, for example, page 1, lines 8 - 10; page 3, lines 17 - 21; page 6, lines 22 - 26; page 9, lines 11 - 13; and page 10, lines 13 - 22. Additionally, claim 1 further requires, among other limitations,

> "compensating for differences in a clock pulse frequency between **the** reference clock pulse and **each** of the data channels using a delay-locked loop circuit" [emphasis added]

Independent claim 8 includes a similar frequency compensation limitation. As claimed in the present application, Applicants' invention generates **a single reference clock pulse**. In the claimed invention, differences in the clock pulse frequency for **each** of the plurality of data channels is compensated based on **the same, generated reference clock pulse** using a delay-locked loop (DLL).

In contrast, the **LEE** reference discloses a DLL in which a phase detector compares the phase of the output of the DLL with that of a reference input. An embodiment of **LEE**, pointed

to in the Office Action, describes the incoming clock signal being processed through a duty cycle corrector which produces an output clock waveform that possesses a 50% duty cycle independent of the input duty cycle. In this embodiment of **LEE**, the duty cycle corrected signal is then input to the phase shifter. However, **LEE** neither teaches, nor suggests, generating a reference clock pulse and applying that reference clock pulse to **each** of a plurality of data channels to compensate for a frequency difference between the each data channel and the reference clock pulse, as presently claimed by Applicants. Rather, the **LEE** reference only describes using **one data input** as shown in Fig. 7a of **LEE**. Nowhere in the **LEE** reference is the use of multiple, unsynchronized inputs contemplated. As such, the **LEE** reference fails to teach or suggest Applicants' invention, as set forth in independent claims 1 and 8, and all claims depending therefrom.

In the Office Action, claim 2 was also rejected based on the **LEE** reference. Applicants additionally traverse this rejection, not only because Applicants believe that claim 1 is patentable over **LEE**, as described above, but because **LEE** also fails to teach or suggest the particular limitation recited in claim 2. Applicants' claim 2 recites, in addition to the limitations of claim 1,

> "deriving the reference clock pulse using a phase-locked loop circuit and data provided by one of the data channels serving as a reference channel."

In the Office Action, it was stated that

> "Lee teaches deriving the reference clock pulse using a phase-locked loop circuit and data provided by one of the data channels serving as a reference channel [*col. 1, lines 13 - 19*]"

However, Applicants respectfully disagree with this statement of the Office Action. Column 1, lines 13 - 19 of the **LEE** reference, state that in the prior art, conventionally, phase locked loops (PLLs) are used to provide the desired clock signal. But **LEE** goes on to diminish the desirability of a PLL in generating the clock signal. See, column 1, lines 19 - 20. **LEE** further goes on to teach the DLL as an alternative to the PLL. See, column 1, lines 29 - 32. As such, Applicants believe that to use the PLL of the prior art to generate the clock signal, in place of the DLL of **LEE** would destroy the teachings of the **LEE** reference.

It is accordingly believed that the **LEE** reference, neither shows nor suggests the features of Applicants' claims. Claims 1 and 8 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on either claim 1 or claim8. As it is believed that the claims were

patentable over the cited art in their original form, they have not been amended herein.

Finally, Applicants appreciatively acknowledge the Examiner's statement that claims 7 and 9 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, Applicants respectfully believe that rewriting of claims 7 and 9 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1 - 17 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Additionally, please consider the present as a petition for a one month extension of time, and please provide a one month extension of time, to and including, Monday, November 15, 2004 to respond to the present Office Action.

The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

KPS:cgm

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